

PCT

世界知的所有権機関
国際事務局
特許協力条約に基づいて公開された国際出願



(51) 国際特許分類6 H04N 5/335	A1	(11) 国際公開番号 WO97/07630												
		(43) 国際公開日 1997年2月27日 (27.02.97)												
<p>(21) 国際出願番号 PCT/JP96/02281</p> <p>(22) 国際出願日 1996年8月12日 (12.08.96)</p> <p>(30) 優先権データ</p> <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 33%;">特願平7/206140</td> <td style="width: 33%;">1995年8月11日 (11.08.95)</td> <td style="width: 33%;">JP</td> </tr> <tr> <td>特願平7/206143</td> <td>1995年8月11日 (11.08.95)</td> <td>JP</td> </tr> <tr> <td>特願平8/53220</td> <td>1996年3月11日 (11.03.96)</td> <td>JP</td> </tr> <tr> <td>特願平8/59845</td> <td>1996年3月15日 (15.03.96)</td> <td>JP</td> </tr> </table> <p>(71) 出願人 (米国を除くすべての指定国について)</p> <p>株式会社 東芝 (KABUSHIKI KAISHA TOSHIBA) [JP/JP] 〒210 神奈川県川崎市幸区堀川町72番地 Kanagawa, (JP)</p> <p>(72) 発明者: および</p> <p>(75) 発明者/出願人 (米国についてのみ)</p> <p>松長義之 (MATSUNAGA, Yoshiyuki) [JP/JP] 〒247 神奈川県横浜市小綱谷1-4-21-212 Kanagawa, (JP)</p> <p>大澤慎治 (OHSAWA, Shinji) [JP/JP] 〒243-04 神奈川県海老名市国分北1-21-24-204 Kanagawa, (JP)</p> <p>中村信男 (NAKAMURA, Nobuo) [JP/JP] 〒183 東京都府中市東芝町2-1-E620 Tokyo, (JP)</p> <p>(31) 指定国 JP, KR, US, 歐州特許 (DE, FI, FR, NL).</p> <p>添付公開審類 国際調査報告書</p>			特願平7/206140	1995年8月11日 (11.08.95)	JP	特願平7/206143	1995年8月11日 (11.08.95)	JP	特願平8/53220	1996年3月11日 (11.03.96)	JP	特願平8/59845	1996年3月15日 (15.03.96)	JP
特願平7/206140	1995年8月11日 (11.08.95)	JP												
特願平7/206143	1995年8月11日 (11.08.95)	JP												
特願平8/53220	1996年3月11日 (11.03.96)	JP												
特願平8/59845	1996年3月15日 (15.03.96)	JP												
<p>(54) Title: MOS IMAGE PICKUP DEVICE</p> <p>(54)発明の名称 MOS型固体撮像装置</p> <p>(57) Abstract</p> <p>A MOS image pickup device in which unit cells are arranged two-dimensionally in a matrix, a horizontal line (column) of unit cells is selected by means of a vertical address circuit, a vertical signal line to which the outputs of one vertical line (row) of unit cells are fed by means of a horizontal address circuit, and the signals of the unit cells are sequentially outputted. Each unit cell is provided with an output circuit which outputs the output of a photodiode to a vertical signal line, a plurality of photodiodes connected in parallel with the output circuit, and selection switch which selects one of the photodiodes and connects the selected photodiodes to the output circuit. The output circuit is composed of an amplifying transistor which amplifies the outputs of the photodiodes, a selection transistor which selects one of the unit cells, and a reset transistor which resets the electric charge of the photodiodes.</p>														

BEST AVAILABLE COPY

WO 97/07630

PCT/JP96/02281

28/29

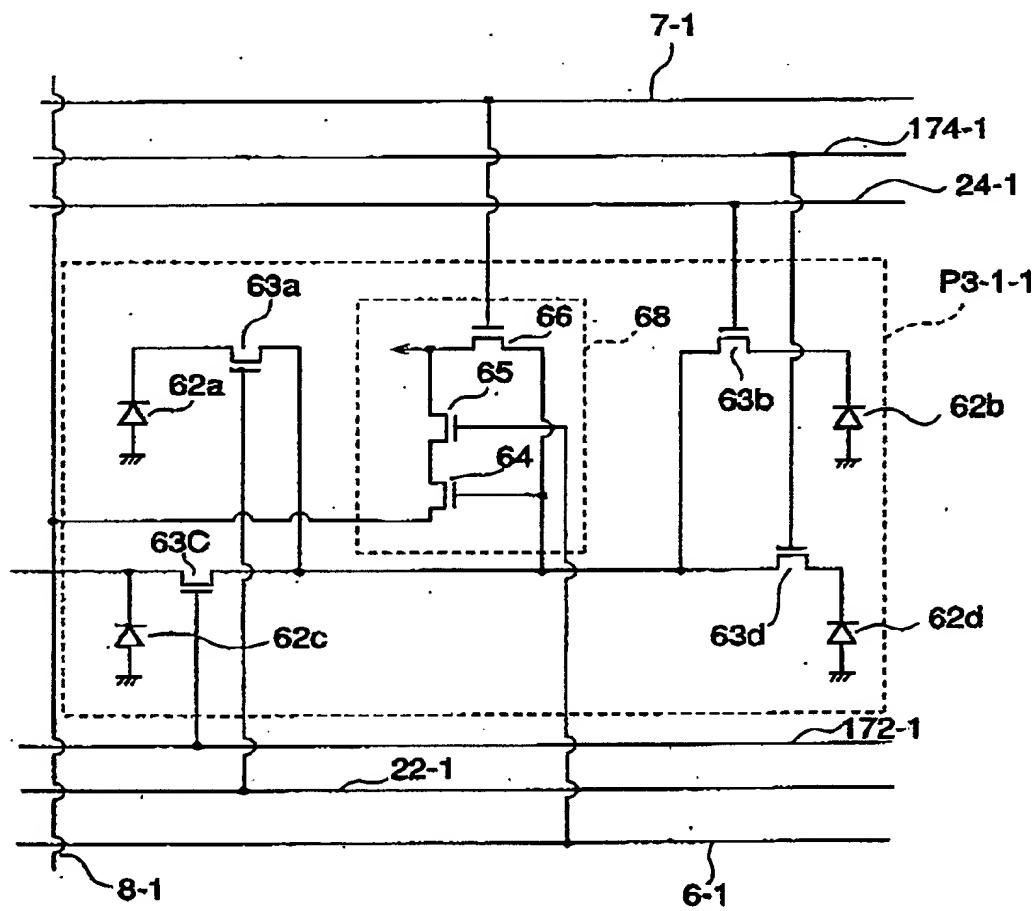


FIG. 33

BEST AVAILABLE COPY

Our translation of page 31, lines 2-17 of the document (2)

Fig. 33 shows a structure of a unit cell P3-1-1 shown in Fig 32. This figure shows only the unit cell P3-1-1. However, each of the other unit cells P3-1-2 etc. has the same structure as the unit cell P3-1-1.

As shown in Fig. 33, a unit cell of a MOS-type solid-state image pickup apparatus of the present embodiment is constructed with four photodiodes 62a to 62d, four photodiode selection transistors 63a to 63d and one output circuit 68. The four photodiodes are arranged in a matrix form of two rows x two columns.

The photodiodes 62a to 62d are connected in common to the output circuit 68 respectively through the selection transistors 63a to 63d. The respective selection transistors 63a to 63d are independently turned on and off via photodiode selection lines 22-1, 24-1, 172-1 and 174-1 which are arranged from a vertical address circuit 5 in a horizontal direction.

As described above, since the unit cell P1-1-1 is constructed by connecting the four photodiodes 62a to 62d in common to the output circuit 64, the present embodiment can omit three output circuits compared with a MOS-type solid-state image pickup apparatus of the prior art.

BEST AVAILABLE COPY